SNP739D8X

Highly integrated tire pressure monitoring sensor

SNP739D8X Datasheet

Release version: Version 1.3

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Consultation Information

For further information on technical support, delivery and prices, please call the national consultation hotline: *021-5061-0206*, or you can obtain relevant support by email *info@senasic.com*.

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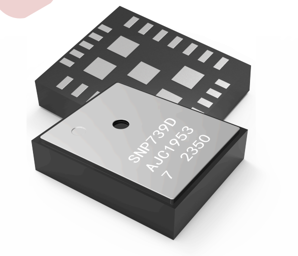
Feature

- Calibrated pressure sensor for absolute pressure measurement with optional measurement range:900kPa/1500kPa
- Temperature and supply voltage sensors
- XZ-axis accelerometer with calibration
- 12-bit analog-to-digital converter (ADC12)
- **RF Transmitter**
  - On chip PA
  - 315/433MHz supported
  - Support ASK/FSK modulation
  - Support Manchester/PWM/Bi-Phase/ Mark-space encoding
- **LF Receiver**
  - Support LF programming
  - 3.9kbps supported
  - Manchester encoding
  - Carrier or telegram wakeup supported
- Support Wheel Auto Mapping (WAM)
- **On chip RC oscillator**
  - 1kHz/4kHz/32kHz/2MHz/4MHz
- **MCU**
  - 8-bit MCU
  - Based on 1T 8051 core
  - 16K Bytes Flash
  - 32K Bytes ROM
  - 512 Bytes data RAM and 128 Bytes retention RAM
  - 6 GPIOs, All GPIOs support low power wakeup
  - SPI/UART/I2C/LIN interface supported
  - Timer 8 with PWM function
- Standby current 0.2μA
- Package: LGA 24pins. 6.0mmx5.0mmx1.9mm

Applications

- Tire Pressure Monitoring sensor
- MEMS sensing

AEC
Q100+125℃



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List of Abbreviations (keyword:TPMS)

Abbreviations	Full Name
PA	Power Amplifier
AON	Always Online
LGA	Land Grid Array
WAM	Wheel Auto Mapping
MCU	Microcontroller Unit
FLASH	Flash Memory
ADC	Analog to Digital Converter
RAM	Random Access Memory
RF	Radio Frequency
LF	Low Frequency
UART	Universal Asynchronous Receiver/Transmitter
SPI	Serial Peripheral Interface
I2C	Inter Integrated Circuit
TPMS	Tire Pressure Monitoring System
MEMS	Micro Electromechanical System
ASK	Amplitude Shift Keying
FSK	Frequency Shift Keying
CRC	Cyclic Redundancy Check
POR	Power On Reset
BOR	Brown Out Reset
XTAL	External Crystal Oscillator
SFR	Special Function Register
IRAM	Internal RAM
XRAM	External RAM
PWM	Pulse Width Modulation
PLL	Phase Locked Loop
CPU	Central Processing Unit

1 Introduction

SNP739D8X consists of 16K Flash memory, 32K ROM memory, interrupt bus, configuration registers and control bus which operate the analogue circuitry all of which are controlled via an 8-bit integrated microcontroller.

The micro is clocked by a tunable oscillator with a selectable center frequency. The motion detection is achieved via accelerometer.

Measurements of pressure, acceleration, temperature, and battery voltage are performed under software control, allowing the application software to format and prepare the data for RF transmission.

A software defined wakeup mechanism is developed for minimizing power consumption. An Interval timer controls the timing of measurements and transmissions.

For smart manage SNP739D8X workload, accelerometer motion and phase location detection integrated in SNP739D8X. And both tire roll status detection and WAM are supported, with no addition accelerometer need.

Embedded LF receiver can help SNP739D8X to wake up at regular intervals and it works independently with no CPU aids at any time of user definition timeout period, thus helps power saving greatly, The LF receiver supports wireless Flash programming to the chip without I2C communication which demonstrates high efficiency in customer firmware development phase. The integrated microcontroller's instruction set is compatible to the standard 8051 processor. It is equipped with hardware Manchester, bi-phase encoder/ decoder and CRC generator and checker, which enable easy implementations of customer specific applications.

The low-power RF Transmitter for 315 and 434 MHz contains a fully integrated PLL synthesizer, an ASK/FSK modulator and an efficient power amplifier.

On-chip Flash memory stores the customer specific application program code, the unique ID-number and the calibration data for the sensor. Additionally, the embedded library functions developed by SENASIC cover standard tasks used by the application.

Table 1 Order Information

Model	Pressure Range	Package	Packing Option
SNP739D81CLE	100 ~ 900	LGA24	3000ea/Reel
SNP739D82CLE	100 ~ 1500		3000ea/Reel

2 Pin Description

Figure 1 Pin Configuration(Top View)

Table 2 Pin Description

Pin No.	Name	Pin Type	Function
1	RESET		Connect to GND
2	LFA	Analog IO	LF channel coil connection
3	LFB	Analog IO	LF channel coil connection
4	TP0		Connect to GND
5	GPIO4	Digital IO	GPIO/SPI MISO/UART RXD
6	GPIO3	Digital IO	GPIO/SPI MOSI/UART TXD
7	GPIO2	Digital IO	GPIO/SPI CSN
8	GPIO1	Digital IO	GPIO/I2C data
9	GPIO0	Digital IO	GPIO/I2C Clock
10	TP1		Connect to GND
11	VREG	Supply	Internal regulator,it must not be used as external current source.
12	GPIO5	Digital IO	GPIO/SPI CLK
13	VSSP	Supply	Ground
14	RF	Analog IO	RF output
15	VDDP	Supply	Battery supply 3V
16	XTAL	Analog IO	XTAL pin
17	VDD	Supply	Battery supply 3V
18	VREF1	Analog IO	100nF to ground
19	NC		N.C.
20	NC		N.C.
21	NC		N.C.
22	NC		Not connect
23	NC		Not connect
24	NC		Not connect
25~29	GND	Supply	Ground

3 Specification

3.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Max.Supply Voltage	V_{DDmax}	-0.3		+3.8	V	
ESD robustness HBM	V_{ESD_HBM}	-2000		+2000	V	All pins according to JS-001-2014
		-4000		+4000	V	RF pin according to JS-001-2014
ESD robustness CDM	V_{ESD_CDM}	-500		+500	V	All pins according to JS-002-2014
		-750		+750	V	Corner pins
Latch up	I_{LU}	-100		+100	mA	All pins according to JEDEC 78D
Input Voltage	V_{in}	-0.3		V_{DD}+0.3	V	GPIO0~GPIO5
		-0.3		V_{DD}+0.3	V	XTAL
		-0.3		V_{DD}+0.3	V	LFA, LFB
Dynamic voltage at RF pin	V_{dyn_PAOUT}			V_{DD} +0.3	V	
DC current	I_{DC}	-10		+10	mA	GPIO0~GPIO5
		-10		+10	mA	XTAL
		-10		+10	mA	LFA, LFB
Input pressure	P_{in}	0		2000	kPa	
		2000		2500	kPa	Maximal 2s 5 times over lifetime
Constant Acceleration	a_{CA}			3500	g	Tested in +/- x,y,z- direction.(Device unpowered)
Mechanical Shock	a_{MS}			10000	g	0.3 ms half sine pulses. 5 shocks in +/- x,y,z-direction,respectively. (Device unpowered)
Variable Frequency Vibration	f_{VFV}	20		2000	Hz	Tested in +/- x,y,z- direction,50 g peak acceleration.
Package Drop	h_{Drop}			1.2	m	Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.

3.2 Operating Range

Table 4 Operating Range

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	2.1	3.0	3.6	V	
Ambient Temperature	$T_{operating}$	-40		125	°C	Normal operation
	T_{Flash}	-40		125	°C	Flash programming/erasing

3.3 Characteristics

3.3.1 Pressure Sensor

Table 5 Pressure Sensor 900kPa Variant

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input Pressure Range	$P_{in,H}$	100		900	kPa	
ADC Resolution	$P_{ADC\_res,H}$			1.1	kPa/LSB	
Random Error	$P_{random,H}$	-2.3		2.3	kPa	95% of all measurements
Measurement Error	$P_{Error\ 100\text{-}500KPA}$	-5		5	kPa	0°C to +70°C
		-10		10	kPa	-40°C to +125°C
	$P_{Error\ 500\text{-}900KPA}$	-7		7	kPa	0°C to +70°C
		-15		15	kPa	-40°C to +125°C

Table 6 Pressure Sensor 1500kPa Variant

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input Pressure Range	$P_{in,H}$	100		1500	kPa	
ADC Resolution	$P_{ADC\_res,H}$			1.6	kPa/LSB	
Random Error	$P_{random,H}$	-3.3		3.3	kPa	95% of all measurements
Measurement Error	$P_{Error\ 100\text{-}500KPA}$	-7		7	kPa	0°C to +70°C
		-12		12	kPa	-40°C to +125°C
	$P_{Error\ 500\text{-}900KPA}$	-10		10	kPa	0°C to +70°C
		-20		20	kPa	-40°C to +125°C
	$P_{Error\ 900\text{-}1200KPA}$	-15		15	kPa	0°C to +70°C
		-30		30	kPa	-40°C to +125°C
	$P_{Error\ 1200\text{-}1500KPA}$	-20		20	kPa	0°C to +70°C
		-20		50	kPa	-40°C to +125°C

3.3.2 x/z-axis Acceleration Sensor

Table 7 x axis Acceleration Sensor

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input acceleration Range	$a_{in,x}$	-120		120	g	
Total Acceleration Error	$a_{err\_tot,x}$	-3		3	g	| a_{in} |<20g,0°C <=T<90°C
		-5		5	g	| a_{in} |<20g,-40°C <=T<125°C
		-8		8	g	20g<=| a_{in} |<100g, 0°C <=T<90°C
		-10		10	g	20g<=| a_{in} |<100g, -40°C <=T<125°C
		-10		10	g	100g<=| a_{in} |<120g, 0°C <=T<90°C
		-12		12	g	100g<=| a_{in} |<120g, -40°C <=T<125°C
Random error	$a_{random,x}$	-0.2		0.2	g	The ADC sets 128 filters
ADC resolution	$a_{ADC\_res,x}$		0.0625		g/LSB	

Table 8 z axis Acceleration Sensor

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input acceleration Range	$a_{in,z}$	-400		400	g	
Total Acceleration Error	$a_{err\_tot,z}$	-3		3	g	| a_{in} |<20g, 0°C <=T<90°C
		-5		5	g	| a_{in} |<20g, 40°C <=T<125°C
		-8		8	g	20g<=| a_{in} |<100g, 0°C <=T<90°C
		-10		10	g	20g<=| a_{in} |<100g, -40°C <=T<125°C
		-18		18	g	100g<=| a_{in} |<200g, 0°C <=T<90°C
		-20		20	g	100g<=| a_{in} |<200g, -40°C <=T<125°C
		-38		38	g	200g<=| ain |<400g, 0°C <=T<90°C
		-40		40	g	200g<=| ain |<400g, -40°C <=T<125°C
Random error	$a_{random,z}$	-0.3		0.3	g	The ADC sets 128 filters
ADC resolution	$a_{ADC\_res,z}$		0.1		g/LSB	

3.3.3 Temperature Sensor

Table 9 Temperature Sensor

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Measurement range	T_{range}	-40		+125	°C	
Measurement error	T_{Error}	-5		+5	°C	-40°C to -20°C,V_{DD}=2.1 to 3.6V
		-3		+3	°C	-20°C to 90°C,V_{DD}=2.1 to 3.6V
		-5		+5	°C	+90°C to +125°C,V_{DD}=2.1 to 3.6V
Random error	T_{random}	-1		+1	°C	

3.3.4 Battery Sensor

Table 10 Battery Sensor

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Measurement range	V_{range}	2.1		3.6	V	
Measurement Error	V_{Error}	-3		+3	%	Percentage of measurement value

3.3.5 Thermal Shutdown

Table 11 Thermal Shutdown

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal Shutdown HOT threshold	$T_{HOT,TH}$	110		120	°C	
Thermal shutdown HOT release	$T_{HOT,RE}$	100		110	°C	
Hysteresis	T_{HYST}		10		°C	

3.3.6 General Purpose Digital I/O Pins

Table 12 Digital I/O Pins - Operating Range

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Digital Pin Output Current	$I_{out\ DIG}$	-4		4	mA	Pins GPIO0~ GPIO5
Digital Pin Input High Voltage	V_{IH}	$0.7V_{DD}$			V	
Digital Pin Input Low Voltage	V_{IL}			$0.3V_{DD}$	V	

Table 13 Digital I/O Pins - Electrical Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Digital Pin-Output High Voltage	V_{OH}	$0.75V_{DD}$			V	at 4 mA load current
Digital Pin-Output Low Voltage	V_{OL}			$0.2V_{DD}$	V	
Digital Pin Input Capacitance	C_{in}		2		pF	

3.3.7 Power On Reset and Battery Monitoring

Table 14 Power On Reset and Battery Monitoring

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Power on Reset level	V_{POR}	1.1		1.8	V	
Power On Reset Release Level	V_{THR}	1.5		2.1	V	
Low Battery Threshold Warning Level	V_{LBAT}	2.2	2.3	2.4	V	Low Battery Threshold is set to 2.3V

3.3.8 FLASH Memory

Table 15 FLASH Memory

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Flash memory data retention time	$t_{Ret\ Flash}$	10			year	Defect rate < 1ppm over lifetime for typical mission temperature profile
Flash write cycles	N_{write}	1000			time	
Flash page write time	t_{write_page}			7.6	ms	Including time for verification. I2C Baud rate = 400 kbit/s

3.3.9 Supply Currents

Table 16 Supply Currents at 3.0V Supply Voltage

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Supply current in Powerdown state	$I_{PWD@1K\_3V}$		0.3	0.7	µA	+25°C
			1.3	3.5	µA	+125°C
			0.55		µA	-40°C
Supply current in CPU idle state	$I_{IDLE@32K\_3V}$		5.7	7.5	µA	+25°C
			22	40	µA	+125°C

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Supply current in Run state	I_{RUN_3V}		0.48	0.55	mA	+25°C
			0.5	0.6	mA	+125°C
			0.49		mA	-40°C
Supply current in Thermal shutdown state	I_{TSHD_3V}		5		μA	+125°C
Supply current in LF carrier detection mode	$I_{LFCDFilter\_3V}$		5.3	6.5	μA	+25°C
			5.6	9.5	μA	+125°C
			5.2		μA	-40°C
Supply current in LF data reception mode	I_{LF_3V}		9.7	13.5	μA	+25°C
			10.2	15.2	μA	+125°C
			9.5		μA	-40°C
Supply current at RF@433MHz - transmission(CW or FSK;CPU off)	I_{RFTX_3V}		6.3	7.2	mA	+25°C @5dBm
			7.9	8.8	mA	+25°C @8dBm
			9.9	11	mA	+25°C @10dBm
			6	6.7	mA	+125°C@5dBm
			7.6	8.3	mA	+125°C@8dBm
			9.6	11	mA	+125°C@10dBm
			7.2		mA	-40°C@5dBm
			9		mA	-40°C@8dBm
			11		mA	-40°C@10dBm

3.3.10 LF Receiver

Table 17 LF Receiver Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
LF Carrier Frequency[1]	f_{LF}	115	125	135	kHz	
LF Data Rate	DR_{LF}		3.9		kHz	
Input differential capacitance	$C_{LF\ diff}$		2		pF	
Input differential resistance	$R_{LF\ diff}$		2.8		MOhm	
LF Receiver settling time after power on	$t_{ON\_Set.}$			6	ms	It is only the establishment time after the LF circuit is enabled, and whether the circuit is successfully activated is related to the test environment and signal
LF Telegram Detection Sensitivity	$S_{nodet.}$	0.5			mVpp	-40°C to +125°C, +2.1V to +3.6V
	$S_{det.}$			8.5	mVpp	-40°C to +125°C, +2.1V to +3.6V
LF Carrier Detection Sensitivity	$S_{nodet.}$	1			mVpp	-40°C to +125°C, +2.1V to +3.6V
	$S_{det.}$			10	mVpp	-40°C to +125°C, +2.1V to +3.6V

Note:
[1] LF sensitivity levels are only valid for the specified carrier

frequency range.

3.3.11 RF Transmitter

Table 18 RF1 Transmitter Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Transmit Frequency	$f_{TX,315M,XTAL}$	314		316	MHz	
	$f_{TX,433M,XTAL}$	433		435	MHz	
Output Power transformed into 50 ohm	$P_{O,L1,433.92MHz}$		5.2		dBm	V_{bat}=3.0V, T=25°C,Z_{load}=50 ohm RF matched Power Level=1
	$P_{O,L2,433.92MHz}$		7.2		dBm	V_{bat}=3.0V, T=25°C,Z_{load}=50 ohm RF matched Power Level=2
	$P_{O,L3,433.92MHz}$		8.2		dBm	V_{bat}=3.0V, T=25°C,Z_{load}=50 ohm RF matched Power Level=3
Output Power change over temp	$dP_{-40°C}$		5.7		dB	V_{bat}=3.0V, T=-40°C
	$dP_{125°C}$		4.1		dB	V_{bat}=3.0V, T=125°C
Output Power change over supply	$dP_{2.1V}$		3.5		dB	V_{bat}=2.1V, T=25°C
	$dP_{3.6V}$		7.2		dB	V_{bat}=3.6V, T=25°C, 10dBm gear
RF Datarate	DR_{RF}			19.6	Kbit/s	Manchester coded
RF Data Rate tolerance	dDR_{RF}	-0.5		+0.5	%	
FSK frequency shift	f_{SHIFT}		±45	±70	KHz	Programmable
RF Data Duty Cycle	$DC_{RF,ASK}$	48	50	52	%	Valid only for ASK or FSK
ASK Mod depth	$MD_{RF,ASK}$	95		99.5	%	

Table 19 RF1 Crystal Oscillator

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Crystal Frequency	f_{XTAL}		24/26		MHz	
Crystal Oscillator driving current	I_{Xtal_drive}	0.25		0.45	mA	
Crystal Oscillator startup time	t_{Xtal_start}			2	ms	

3.3.12 up and power-on timing

Table 20 up and power-on timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Power on time	t_{ini}			10	ms	From the power on to the user program began to run
Resume from System idle time	t_{resume}			400	μs	Time from resume event during system-idle to application code execution start.
LF Wake-up time	$t_{LF\ wake\text{-}up}$			2.5	ms	Time from LF wake-up event during power-down to application code execution start.

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Watchdog Wake-up time	$t_{wd\ wake\text{-}up}$			600	µs	Time from watchdog timer elapsed during power-down to application code execution start.

3.3.13 Typical Clock and Typical Clock Deviation

Table 21 Typical Clock

Parameter	Symbol	Clock	Values			Unit	Note/Test Condition
			Min.	Typ.	Max.		
Typical clock	I_{clock_3V}	2M		2		MHz	+25°C
		4M		4		MHz	+25°C
		125K		125		KHz	+25°C
		32K		32		KHz	+25°C
		4K		4		KHz	+25°C

Note:
Data in the table are calibrated values.

Table 22 RC Oscillator Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature drift of 2MHz oscillator	TD2M			0.16	%/°C	
Total tolerance of 2MHz oscillator	TOL2M	-10		10	%	-40 to 125°C
Temperature drift of 4MHz oscillator	TD4M			0.2	%/°C	
Total tolerance of 4MHz oscillator	TOL4M	-20		20	%	-40 to 125°C
Temperature drift of 125KHz oscillator	TD125K	-0.5		0.5	%/°C	
Total tolerance of 125KHz oscillator	TOL125K	-5		5	%	-40 to 125°C
Temperature drift of 32KHz oscillator	TD32K			0.2	%/°C	
Total tolerance of 32KHz oscillator	TOL32K	-20		20	%	-40 to 125°C
Temperature drift of 4KHz oscillator	TD4K			0.2	%/°C	
Total tolerance of 4KHz oscillator	TOL4K	-20		20	%	-40 to 125°C

4 Operating Modes and States

4.1 Device states

In normal operation mode the SNP739D8X can be switched into several device states which differ in the number of enabled circuit blocks. For lowest power consumption unused blocks are disconnected from power supply, hence not even idle currents remain.

Table 23 Device states overview

Device state	Short description	Important activated blocks
Init	Enter Init state when system reset is active.	See Table 4-3 Power management
Run	Application code execution.	See Table 4-3 Power management
CPU idle	CPU clock is stopped to reduce the current consumption, any peripheral interrupt, such as Timer1/Timer2/Timer3/Timer8/SPI/ I2C/UART, ADC, RF Transmitter or LF receiver can wakeup CPU to Run state.	See Table 4-3 Power management
Powerdown	No code execution. Device is waiting for a wake-up event. Lowest current consumption.	See Table 4-3 Power management
Thermal shutdown	Once the system enters Shutdown state it would resume running only when the TMAX circuit temperature is below TMAX threshold setting first, then wake-up timer reset is active.	See Table 4-3 Power management

Table 24 Power management

Block Name	Run	CPU Idle	Powerdown/Shutdown
POR	Active	Active	Active
Low battery monitor	Active	Inactive/Active (Selectable)	Inactive
TMAX detector	Inactive/Active (Selectable)	Inactive/Active (Selectable)	Inactive/Active (Selectable)
Voltage regulator	Active	Active	Inactive
Power management/wake-up timer	Active	Active	Active
CPU	Active	Inactive	No supply
Peripheral CRC, I2C,SPI, LIN, UART,LF decoder, RF encoder	Active	Inactive/Active (Selectable)	No supply
Timer 1,2,3,8	Active	Inactive/Active (Selectable)	No supply
256 Bytes IRAM	Active	Inactive	No supply
128 Bytes XRAM_AON	Active	Inactive	Inactive
FLASH	Active	Inactive	No supply
256 Bytes XRAM	Active	Inactive	No supply
ROM	Active	Inactive	No supply
Crystal oscillator (24MHz/16MHz/26MHz)	Active	Inactive/Active (Selectable)	No supply
1k/4k/32k/125kHz RC oscillator	Active	Active	Active
2MHz/4MHz RC oscillator	Active	Inactive/Active (Selectable)	Inactive
LF interval timer	Active	Inactive/Active (Selectable)	Inactive/Active (Selectable)
LF receiver	Active	Inactive/Active	Inactive/Active

Block Name	Run	CPU Idle	Powerdown/Shutdown
		(Selectable)	(Selectable)
RF transmitter	Active	Inactive/Active (Selectable)	No supply

Note: **Active**: block is powered, active and keeps its register contents; **Inactive**: block is powered, cannot be used, but keeps it register contents;**No supply**: block is not powered, cannot be used and all register content is lost.

4.2 State Transitions

Figure 2 shows the possible state transitions in normal mode. The central device state is Run state because only in Run state the state transitions can be configured. Entering other states from Run state is controlled by application code, either by calling firmware functions or setting control bits. State transitions from other states are controlled by hardware events, e.g. timer events or LF receiver events.

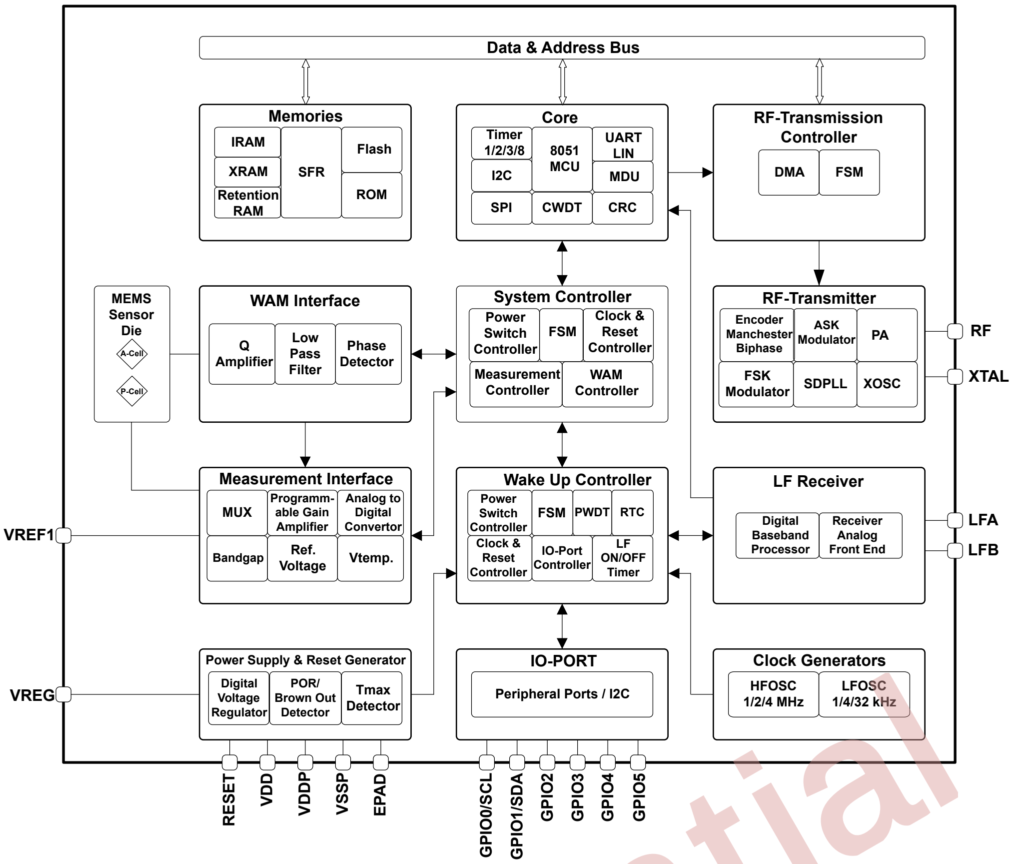
Figure 2 State transitions

Note:
The system can be wakeup from CPU idle to Run state by any interrupt.

5 Functional Descriptions

5.1 Block Diagram

Figure 3 Block Diagram



5.2 up Controller

In a typical TPMS application the SNP739D8X is in Powerdown state most of its lifetime. In Powerdown state, which is triggered by setting register PCON[bit7] to 1, the device is controlled only by the wake-up controller. The wake-up controller is the block with highest priority in terms of power management. It is always powered and waits for a wake-up event from different sources. For lowest power consumption the wake-up controller is clocked by the 1kHz oscillator. If a wake-up event happens and the event is not masked then the wake-up controller powers on the system controller which takes over device control. Before code execution starts the CPU runs a firmware boot sequence and all registers are initialized with their wake-up values. In the case of normal mode the time from wake-up event occurrence until start of application code execution is in the range of several milliseconds. The implemented wake-up sources are:

- Period Wakeup timer (RTC)
- LF-Receiver: carrier detector
- LF-Receiver: wakeup ID matching circuit

- LF-Receiver: sync head detection
- General purpose I/O (GPIO0~GPIO5 configurable)
- TMAX detector when device is in Thermal shutdown

The second main function of the wake-up controller is reset handling. The reset signals are generated in the block “power supply and reset generator”. A system-reset may be trigged by:

- Brown out (internal regulated voltage drops below a certain threshold)
- Power on
- Software
- Period wakeup timer underflow

When Power on reset or Brown out reset occurs, all logic will be reset. After reset release, the chip work mode will be decided by the value of GPIO0 and GPIO1(see Charpter 4.1). Period wakeup timer reset and software reset will not change chip work mode selection.

Furthermore, the wake-up controller comprises the LF ON-OFF timer that allows operating the LF-receiver with a configurable duty cycle for power saving reasons.

5.2.1 Period wakeup Timer (RTC)

The period wakeup Timer is a 16-bit timer (SFRs RTCH and RTCL). The main function is to periodically wake-up the device from power down. The timer is active in any low power state and is clocked by the 1kHz oscillator. The PWDT is counting down, a wake-up event is triggered upon timer underflow. The PWDT should be properly configured to avoid interrupting the telegram transmission or the data acquisition.

The associated registers are:

- RTCH, RTCL: wakeup timer counter
- RTCCON: wakeup timer control register

5.2.2 LF ON-OFF Timer

The function of the on-off timer is to realize the switch of LF receiver ON/OFF to save power consumption. By configuring register LFCON1 to set the open and close, The opening time can match for 1/2/4/8/16/32/64/128/256/512/1024 ms, the closing time can match for 8/16/32/64/128/256/512/1024/2048/4096 ms. By setting LFSTM to 0xF, the system can be configured to be in continuous ON mode.

Setting bits LF_WAKE_EN activates the ON-OFF timer. The current count value of the ON-OFF timer cannot be read by software.

Associated registers:

- LFCON1, bits LFSTM and LFONTM
- PCON, bit LF_WAKE_EN

5.2.3 LF Receiver Wake-up/Resume Events

The LF receiver wake-up events are:

- Carrier detected
- Wake-up pattern match
- Sync head detection

5.2.4 General Purpose I/O Wake-up/Resume Event

All I/O Ports (GPIO0~GPIO5) can be configured as an external wake-up source. In order to use this wake-up source, the corresponding GPIO needs to be configured as input (SFR bits GPIO0DIR~GPIO5DIR=1), the corresponding pull resistor must be enabled (SFR bits GPIO0_PUPD~GPIO5_PUPD=0) and the corresponding wake-up must be enabled (SFR bits IO0_WAKE_FLAG_EN=1 and IO1_WAKE_FLAG_EN=1) and the corresponding wake-up I/O must be selected(WAKE_IO_SEL[1:0]).

Note:
Note that the General purpose I/O wake-up is triggered on low level only.

Table 25 Truth Table of Wake-Up I/O Selection

GPIOnDIR	GPIOn_PUPD	GPIOnOUT	IO0_WAKE_FLAG_EN (GPIODIR[7])	IO1_WAKE_FLAG_EN (GPIODIR[6])	WAKE_IO_SEL[1:0] (GPIODATN[7:6) (GPIODATN[7:6) RFCNT1H[3:2]RFCNT1H[3:2]	Selected wake-up I/O
1	0	1	0	0	Ignore	Disable
1	0	1	0	1	00	GPIO2
1	0	1	0	1	01	GPIO3
1	0	1	0	1	10	GPIO5
1	0	1	0	1	11	GPIO2 GPIO3 GPIO5
1	0	1	1	0	00	GPIO0
1	0	1	1	0	01	GPIO1
1	0	1	1	0	10	GPIO4
1	0	1	1	0	11	GPIO0 GPIO1 GPIO5
1	0	1	1	1	00	GPIO0 GPIO2
1	0	1	1	1	01	GPIO1 GPIO3
1	0	1	1	1	10	GPIO4 GPIO5
1	0	1	1	1	11	GPIO0~ GPIO5

Associated registers:

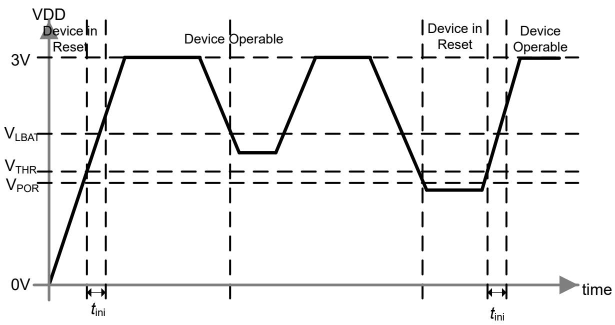
- GPIODIR, GPIO input or output selection
- GPIOPUPD, GPIO wake-up enable and pullup/pulldown selection

- GPIODATN, bits WAKE_IO_SEL[1:0], Wake-up I/O selection

5.2.5 On and Under-Voltage Reset

Figure 4 shows the device behavior depending on voltage at VDD pin. If the voltage falls below a certain threshold V_{POR} a system-reset is triggered. The device stays in reset until the voltage at VDD pin exceeds the reset release threshold V_{THR}. After reset release the device initialization is started which takes a certain time, t_{ini}. After the initialization phase the operation mode of the device can be selected by strapping the GPIO0 and GPIO1.

Figure 4 Power-On and Under-Voltage Reset Behavior



5.2.6 Software Reset

After a reset triggered by software the device runs through the reset boot sequence. The software reset can be triggered by setting the bit RESET (located in register EPCON) in application code. Software reset mainly focus on reset in Normal mode or Debug mode, and it will reset Core and System Controller block, and the chip mode selection is not affected.

Associated registers:

- EPCON(bit RESET for triggering software reset)

5.2.7 Thermal Shutdown

Thermal shutdown function is enabled by setting the bit TSHDWN_EN (located in register PCON) in application code, and the TMAX detector is active when TSHDWN_EN=1. A flag TEMP_ALARM_INT (location in register INTL) is clear if the temperature is below the hot temperature threshold Thot_th. If the temperature is above hot temperature threshold Thot_th, the flag TEMP_ALARM_INT is set 1 by TMAX detector, so the application code can polling the flag TEMP_ALARM_INT, then enter Thermal shutdown by setting the bit PDWN(location in register PCON). Once in Thermal shutdown mode, the device is only release if the on-chip TMAX detector indicates a temperature below the hot release temperature Thot_re. After release from Thermal shutdown a wake-up is performed.

Associated registers:

- EPCON (bit TGOOD for indicating TMAX detector)
- PCON (bit TSHDWN_EN for enable TMAX detector, bit PDWN for enter Thermal shutdown)

5.3 System Controller

Main function of the system controller is power management after device wake-up from power-down or device resume from CPU idle. Unlike the wake-up controller most other circuits can be disconnected from power individually. Depending on the device state the system controller connects the required blocks to the power domain. Here the device states are listed, ordered by current consumption, starting with the state with highest current consumption:

- Run state
- CPU idle state (Run state with CPU disconnected from system clock)
- Powerdown state (optional with LF receiver enabled)

5.3.1 Measurement Controller

Refer to the associated firmware function:

- TPMS_READ_VOLTAGE()
- TPMS_COMP_VOLTAGE()
- TPMS_READ_TEMPERATURE()
- TPMS_COMP_TEMPERATURE()
- TPMS_READ_ACCEL_X()
- TPMS_COMP_ACCEL_X()
- TPMS_READ_ACCEL_Z()
- TPMS_COMP_ACCEL_Z()

5.3.2 WAM Controller

Refer to the associated firmware function:

- WamB_Init()
- WamB_On()
- WamB_Off()
- WamB_GetFiltCycle()

5.4 Clock Generators

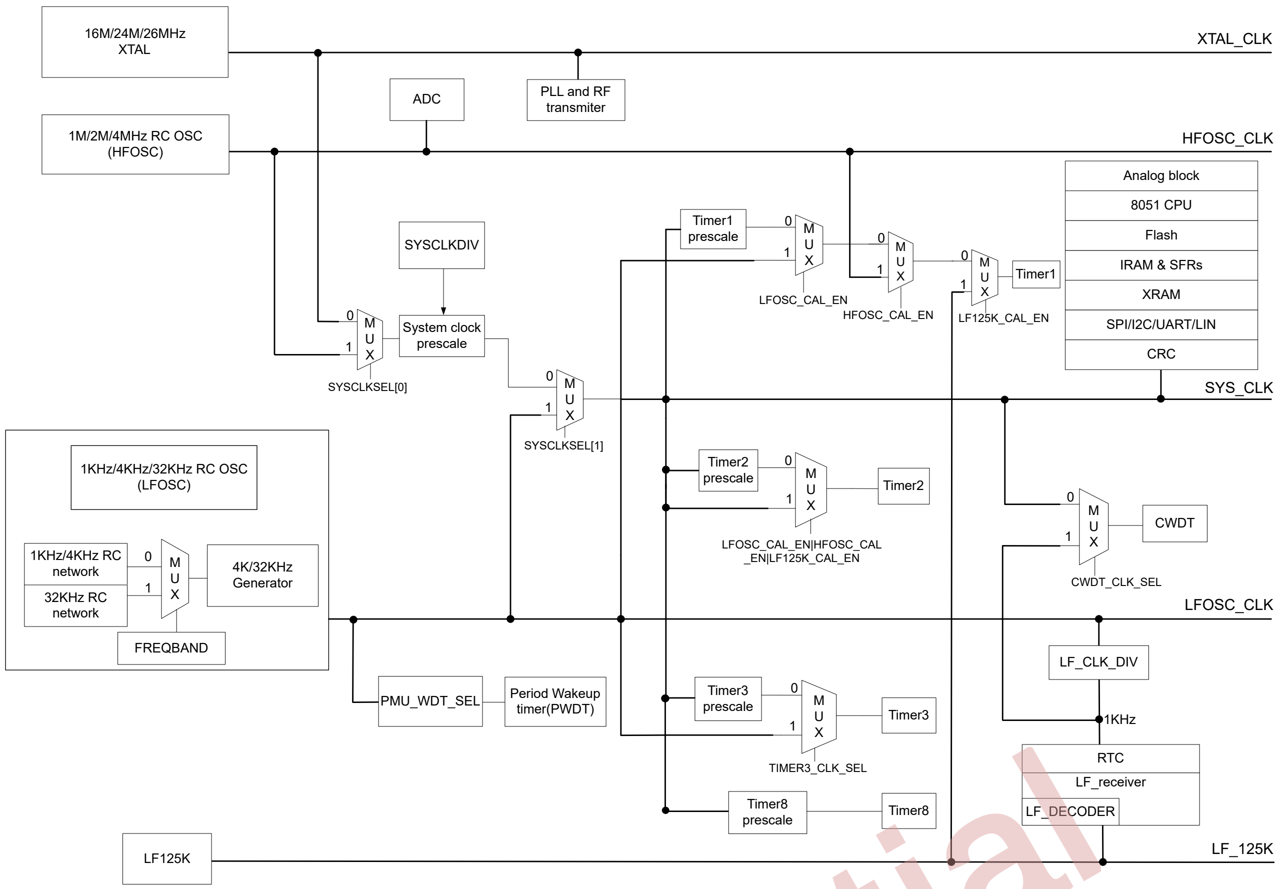
The SNP739D8X has a RC high frequency oscillator (HFOSC) and a RC low frequency oscillator (LFOSC), where the high frequency oscillator can produce a 1MHz/2MHz/4MHz clock signal and the low frequency oscillator can produce a 1KHz/4KHz/32KHz/125KHz clock signal.

2MHz/4M is used for the ADC and system clock, and 1MHz/2MHz/4MHz can also be used as the system clock. 1KHz is used for low frequency modules and watchdog timers, 1KHz/4KHz/32KHz can also be used as a system clock, and 125KHz is used for low frequency modules.

RC high frequency and low frequency oscillators are affected by temperature and voltage, and need to be calibrated periodically to ensure the accuracy of the device.

For RF transmission and calibration purposes a crystal oscillator (XTAL) is implemented as well. The XTAL can also used as system clock by configuring the SFR bits SYSCLKSEL and can be divided by configuring the SFR bits SYSCLKDIV.

Figure 5 Clock distribution diagram.



Associated registers:

- SYSCLKSEL (system clock selection)
- SYSCLKDIV (XTAL or RC OSC 2MHz clock division)

Related firmware functions::

- TPMS_4_CLK_CAL()
- TPMS_32_CLK_CAL()
- TPMS_LF125_CLK_CAL()
- TPMS_2M_CLK_CAL()
- TPMS_4M_CLK_CAL()
- TPMS_SYSCLK_SEL()

5.5 Power Supply and Reset Generator

The Power Supply and Reset Generator provides the power for different voltage domains:

- Analog domain
- Digital domain
- Retention RAM

Furthermore, this functional block provides a reset signal on power-on and under-voltage for the wake-up controller (see Chapter 5.2.5).

Note:
A external capacitor must be connected to VDDREG-pin in order to stabilize the internal voltage. This pin must not be used as voltage supply for external devices.

5.6 Measurement Interface

The measurement interface block is the interface between the analog sensor signals and the digital signal conditioning domain. A multiplexer selects one of the following input signals for the 12-bit analog to digital converter:

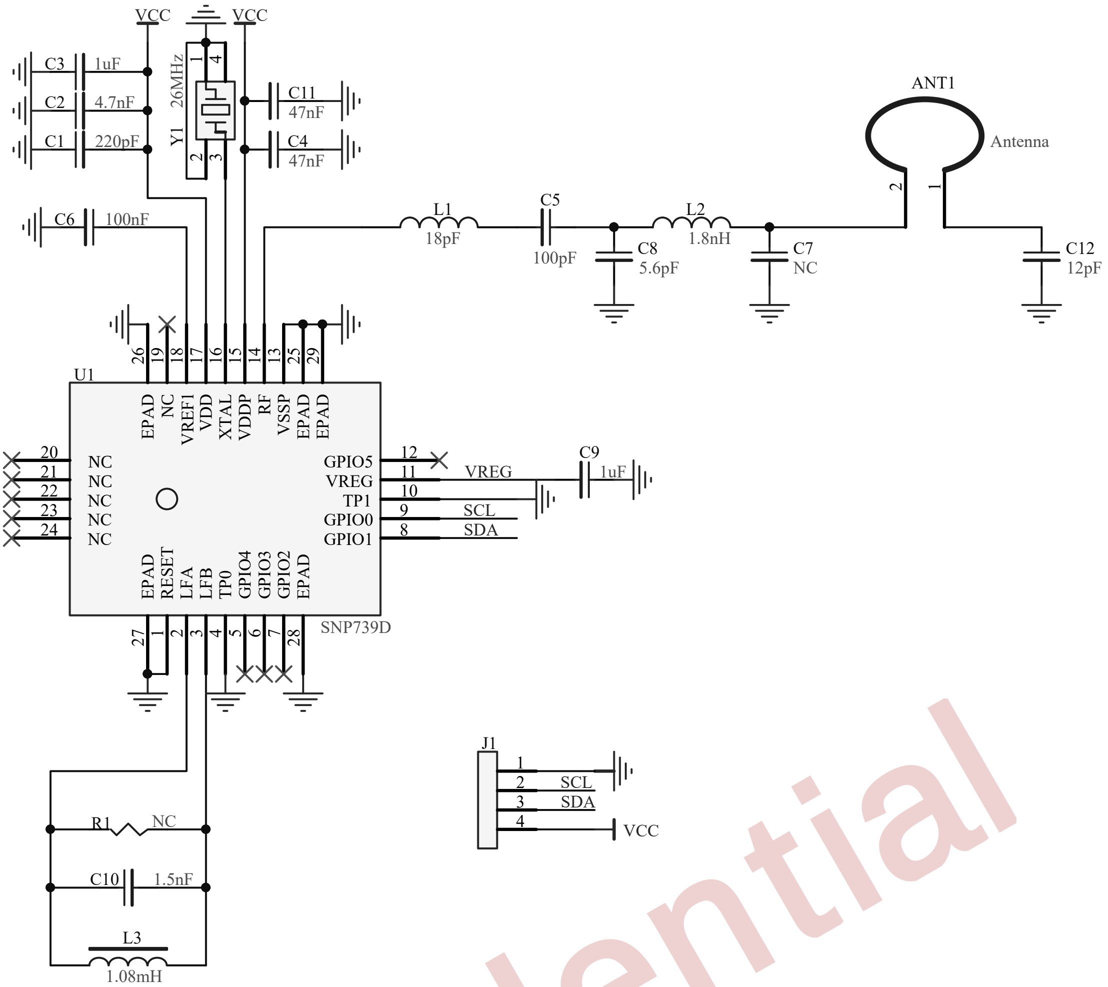
- Pressure Sensor (located on separate MEMS chip)
- Accelerometer (located on separate MEMS chip)
- Temperature Sensor
- Battery Voltage Sensor

5.7 RF Transmission Controller

The RF transmission controller is a state machine (FSM) for handling RF transmission without CPU support. The payload of the RF telegram needs to be generated in application code and stored in the XRAM band addresses 0x6100 to 0x61FF, total 256 bytes. Then the RF transmission controller will be enabled and the device will be switched into system idle state for power saving. The CPU is halted/paused, while the RF state machine directly accesses to the RAM, and automatically transfers the data bytes of the payload to the manchester/PWM encoder. The RF transmission controller also carries out the power management for RF transmission by controlling the PLL circuit, the crystal oscillator and the encoder.

6 Application Circuit

Figure 6 Application Circuit



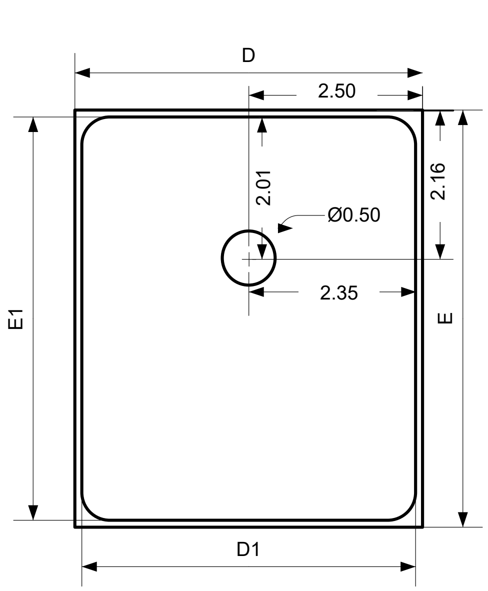
Note:

L1/C5/C8/L2/C7/C12 value might be changed according to different antenna.

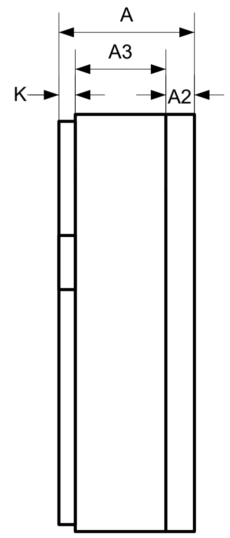
7 Package Information

7.1 Package Outline

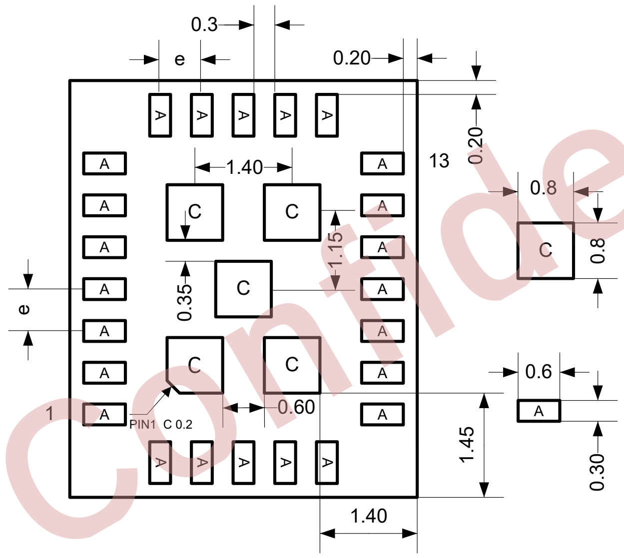
Figure 7 Package Outline



TOP VIEW



SIDE VIEW

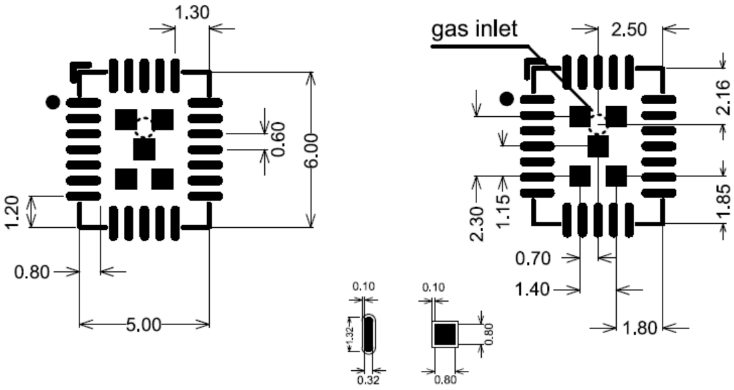


BOTTOM VIEW

	MILLIMETER		
SYMBOL	MIN	NOR	MAX
A	1.75	1.85	1.95
A2	0.27	0.32	0.37
A3	1.33	1.38	1.43
K	0.12	0.15	0.18
D	4.90	5.00	5.10
D1	4.67	4.70	4.73
E	5.90	6.00	6.10
E1	5.67	5.70	5.73
e	BSC 0.6		

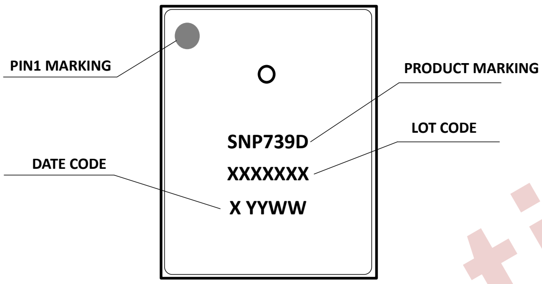
7.2 Footprint

Figure 8 Recommend footprint layout



7.3 Marking

Figure 9 Marking information

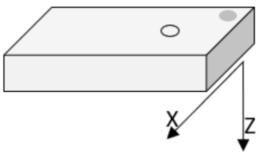


Note:

1.DATE CODE, the first X is either 7 or 9, 7 representing 900kPa and 9 representing 1500kPa, YY representing year (When YY are "24", means 2024), WW representing week (When WW are "09", means the 9th week of the year).

7.4 Accelerometer

Figure 10 Acceleration sensor direction



8 Revision History

Table 26 Revision History

VERSION	DATE	NOTE
V0.1	2024/03/14	Initial version
V1.0	2024/04/05	Fix some error, release version
V1.1	2024/11/08	Update specification data
V1.2	2025/06/24	Recommend modifying the crystal oscillator to 26M.
V1.3	2025/09/12	Fix some error